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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,143	03/19/2004	Shuji Kondo	L8462.04110	6377

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EXAMINER	
CONNOLLY, MARK A	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 07/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,143	KONDO, SHUJI	
	Examiner	Art Unit	
	Mark Connolly	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☒ Claim(s) *7-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 have been presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson US Pat No 5825674.

4. Referring to claim 1, Jackson teaches the invention substantially including:

a. a processor receiving as a system clock a clock signal corresponding to frequency information among a plurality of clock signals of different frequencies that are each 1/n of an oscillation frequency, performing fetching and decoding of an operation code and operand stored in a memory, on an instruction program comprising the operation code and the operand, and executing the instruction program based on a result of the decoding [abstract, col. 3 lines 15-22 and col. 9 lines 6-55]. In particular, a NOP instruction is decoded and identified as a frequency adjustment instruction which then uses a decoded reserved field which is interpreted as an operand since it comprises data used by the NOP instruction to adjust the clock frequency.

b. wherein the operation code, to which a frequency control signal for determining the division ratio of the system clock is added, is stored in the memory [col. 3 lines 13-15].

c. wherein the processor outputs the frequency information corresponding to the frequency control signal by fetching and decoding the frequency control signal together with the operation code [abstract, col. 3 lines 15-22 and col. 9 lines 6-55].

Although Jackson teaches fetching and decoding instructions for controlling the frequency of a processor, it is not explicitly taught that the instructions are fetched and decoded by a pipeline processor. Pipeline processors are well known in the art and it would have been obvious to use a pipeline processor as CPU 110 because pipelined processors provide increased throughput by executing instructions faster than a non-pipelined processor.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson as applied above and further in view of Narayan et al. [Narayan] US Pat No 5940602.

6. Referring to claim 2, Jackson teaches the invention substantially including:

d. a processor receiving as a system clock a clock signal corresponding to frequency information among a plurality of clock signals of different frequencies that are each 1/n of an oscillation frequency, performing fetching and decoding of an operation code and operand stored in a memory, on an instruction program comprising the operation code and the operand, and executing the instruction program based on a result of the decoding [abstract, col. 3 lines 15-22 and col. 9 lines 6-55]. In particular, a NOP instruction is decoded and identified as a frequency adjustment instruction, which then uses a decoded reserved field which is interpreted as an operand since it comprises data used by the NOP instruction to adjust the clock frequency.

e. wherein the operation code, to which a frequency control signal for determining the division ratio of the system clock is added, is stored in the memory [col. 3 lines 13-15].

f. wherein the processor outputs the frequency information corresponding to the frequency control signal by fetching and decoding the frequency control signal together with the operation code [abstract, col. 3 lines 15-22 and col. 9 lines 6-55].

Although Jackson teaches fetching and decoding instructions for controlling the frequency of a processor, it is not explicitly taught that the instructions are fetched and decoded by a pipeline processor. Pipeline processors are well known in the art and it would have been obvious to use a pipeline processor as CPU 110 because pipelined processors provide increased throughput by executing instructions faster than a non-pipelined processor.

In addition, Jackson does not teach that the frequency adjustment instructions comprise an extension code. Narayan teaches an x86 architecture that comprise variable length instruction sets requiring a start bit (interpreted as an extension code) which represents the start of an instruction and an end bit which represents the end of an instruction. It would have been obvious to include the teachings of Jackson into other instruction set architectures such as the x86 architecture, rather than limit it to just a single set, because it would provide additional the same power savings to other different instruction set architectures.

7. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson as applied to claim 1 above, and further in view of Nomura et al [Nomura] US Pat No 6941485.

8. Referring to claims 3 and 5, although Jackson teaches adjusting a clock frequency, it is not explicitly taught how a clock frequency being supplied to a processor is generated and applied. Nomura teaches a means to generate and apply different frequency clocks by dividing a primary clock by a plurality of division ratios and selecting one of the divided clocks to be applied to a processing circuit [figs. 5-6, abstract and co. 12 lines 39-41]. It would have been obvious to one of ordinary to one of ordinary skill in the art at the time of the invention to include the teachings of Nomura into the Jackson system because it provides a means to generate the different frequency clock signals to be applied to the processor.

9. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson and Narayan as applied to claim 1 above, and further in view of Nomura et al [Nomura] US Pat No 6941485.

10. Referring to claims 3 and 5, although Jackson teaches adjusting a clock frequency, it is not explicitly taught how a clock frequency being supplied to a processor is generated and applied. Nomura teaches a means to generate and apply different frequency clocks by dividing a primary clock by a plurality of division ratios and selecting one of the divided clocks to be applied to a processing circuit [figs. 5-6, abstract and co. 12 lines 39-41]. It would have been obvious to one of ordinary to one of ordinary skill in the art at the time of the invention to include the teachings of Nomura into the Jackson-Narayan system because it provides a means to generate the different frequency clock signals to be applied to the processor.

Conclusion

11. Claims 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (571) 272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mark Connolly
Examiner
Art Unit 2115

mc
July 10, 2006

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100